

1 Three Terminal Edge Illuminated Epilayer Waveguide
2 Phototransistor

3
4 FIELD OF THE INVENTION

5
6 This invention relates to phototransistors.

7
8 More particularly, the present invention relates to three
9 terminal edge illuminated heterojunction bipolar
10 phototransistors (HBPTs).

11
12 BACKGROUND OF THE INVENTION

13
14 As the bit rates of telecommunication and data
15 communication systems increase, the demands on the performance
16 requirements of photoreceivers increases. As bit rates extend
17 beyond 40 Gbit/s, the sensitivity of optical receivers tends to
18 decrease causing degradation in the overall performance of the
19 optical communications link. Receiver sensitivity has been
20 improved in prior art by implementing avalanche photodetectors
21 (APDs) as the optical detection element. This improvement in
22 receiver sensitivity has been due to the fact that APDs can
23 provide internal optical to electrical gain through the
24 avalanche multiplication process. Some of the problems
25 associated with implementing APDs in the receiver circuits are
26 that the avalanche multiplication process is an inherently

1 noisy process and requires excessively high bias voltages on
2 the order of 40 volts to achieve the desired gain. The high
3 electric fields that result from these excessively high bias
4 voltages lead to reliability problems that cause premature
5 failure. Many engineering solutions need to be implemented to
6 circumvent these issues. As such, the fabrication and device
7 layer profile are highly specialized for the APD, which
8 prevents the monolithic integration of the APD with the
9 transimpedance amplifier (TIA) circuit. The resulting
10 consequence of this specialization is that it is unlikely that
11 front-end optical receivers that are based on APDs will be able
12 to operate at 40 Gbps bit rates or beyond due to the excessive
13 parasitic losses that come from the hybrid integration of the
14 APD with the rest of the circuit.

15
16 What is desired at these high bit rates is a solution that
17 can improve the sensitivity of the receiver by providing
18 internal optical to electrical gain without the excessive noise
19 characteristics of the APD and without the excessive bias
20 voltages. In addition, a detector that can be easily
21 monolithically integrated with the rest of the receiver
22 electronics would greatly reduce the parasitic losses
23 associated with a hybrid interconnection and further increase
24 the performance of the receiver.

1 It would be highly advantageous, therefore, to remedy the
2 foregoing and other deficiencies inherent in the prior art.

3

4 Accordingly, it is an object of the present invention to
5 provide a new and improved three terminal edge illuminated
6 heterojunction bipolar phototransistor.

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8 It is an object of the present invention to provide a new
9 and improved three terminal edge illuminated heterojunction
10 bipolar phototransistor which decreases the excessive parasitic
11 losses.

12

13 It is another object of the present invention to provide a
14 new and improved three terminal edge illuminated heterojunction
15 bipolar phototransistor which allows it to be monolithically
16 integrated with the receiver circuitry.

17

18 It is another object of the present invention to provide a
19 new and improved three terminal edge illuminated heterojunction
20 bipolar phototransistor which has a short carrier transit-time.

21

22 And another object of the invention is to provide a new
23 and improved three terminal edge illuminated heterojunction
24 bipolar phototransistor which has a high internal quantum
25 efficiency.

1 Still another object of the present invention is to
2 provide a new and improved three terminal edge illuminated
3 heterojunction bipolar phototransistor which has a high
4 external coupling efficiency.

5

6 A further object of the invention is to provide a new and
7 improved three terminal edge illuminated heterojunction bipolar
8 phototransistor which has the ability to perform at bit rates
9 greater than 40 Gbits/second.

SUMMARY OF THE INVENTION

To achieve the objects and advantages specified above and others, an edge illuminated epilayer waveguide phototransistor (hereinafter referred to as "WPT") is disclosed which includes a subcollector layer formed from an epitaxially grown quaternary semiconductor material that is grown on a semiconductor substrate. The epitaxially grown quaternary semiconductor material improves the optical waveguide mode properties. A collector region is epitaxially grown on the subcollector layer. A base region is epitaxially grown on the collector layer. A very thin spacer layer is grown between the base and emitter layers. An emitter region is then epitaxially grown on the spacer layer. The various layers and regions are formed so as to define an edge-illuminated facet for receiving incident light. Further, ohmic contacts are formed to the subcollector, base, and emitter regions to allow electrical signals to be extracted from the phototransistor.

In a preferred embodiment, the subcollector region consists of an InGaAsP quaternary semiconductor with a composition that corresponds to a bandgap wavelength of 1.15 μm . The InGaAsP subcollector is a unique advantage that allows the optimization of the input optical coupling efficiency without sacrificing the phototransistor's electrical performance. The InGaAsP subcollector expands the optical mode

1 in the vertical direction, which increases the input mode
2 coupling efficiency to commercially available lensed optical
3 fibers without degrading the electrical properties of the
4 device. The heavily doped InGaAsP subcollector also maintains
5 the necessary electrical characteristics needed for high
6 performance device operation.

7

8 The WPT discussed here will eliminate all of the
9 previously mentioned issues associated with the APD due to
10 superior noise performance and reduced bias voltage requirement
11 (2 volts). In addition, by optimizing the layer structure of
12 the WPT, the device can be monolithically integrated with
13 receiver circuits consisting of InP-based HBTs resulting in a
14 low-cost, high performance receiver. This is due to the fact
15 that the epilayer profile can be defined to simultaneously
16 optimize the performance of the WPT and the HBT on the same
17 wafer. Also, the WPT uses a subcollector region that expands
18 the optical mode size vertically without degrading the
19 electrical properties of the device. Expanding the optical
20 mode size in this manner increases the input optical coupling
21 efficiency.

22

23 The WPT geometry has inherent advantages over top-
24 illuminated phototransistors that have been demonstrated in the
25 prior art. Some problems associated with the top-illuminated
26 approach include the fact that the thickness of the absorbing

1 layers must be increased to above 1 μm in order to absorb
2 greater than 90% of the incident light. This leads to poor
3 frequency response of the top-illuminated phototransistor due
4 to the excessive base and collector carrier transit-times. The
5 waveguide phototransistor geometry solves this problem because
6 the light propagates and gets absorbed down the length of the
7 device in a direction that is orthogonal to the flow of
8 electrical carriers. As such, the thickness of the absorbing
9 layers can be kept small such that the base and collector
10 transit-times are short which allows for high-speed operation.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and further and more specific objects and advantages of the instant invention will become readily apparent to those skilled in the art from the following detailed description of a preferred embodiment thereof taken in conjunction with the drawings, in which the single figure is a isometric view of a three terminal edge illuminated epilayer waveguide phototransistor in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Turn now to the drawing which illustrates an isometric cross sectional view of a three terminal edge illuminated epilayer waveguide phototransistor 5 in accordance with the present invention. Three terminal edge illuminated epilayer waveguide phototransistor 5 includes a substrate 10 which in this embodiment is formed of semi-insulating InP. It will be understood that the substrate 10 can be any convenient material that is compatible with layers subsequently grown thereon. A buffer layer 20 can be included to provide a pristine surface onto which the device structure can be grown with minimal defects. In this preferred embodiment the buffer layer 20 is composed of InP and is approximately 0.1 μm thick. It will be understood that buffer the layer 20 can be the same material as the substrate 10 or can be composed of an alloy to allow lattice matching to subsequent layers grown thereon. A subcollector layer 30 is then epitaxially grown on area 20. In this preferred embodiment, the subcollector layer 30 consists of a heavily *n*-type doped InGaAsP quaternary alloy with a composition that corresponds to a bandgap wavelength of 1.15 μm . The alloy composition of the InGaAsP quaternary is chosen so that it is transparent to the optical wavelengths of interest. It will be understood that subcollector layer 30 can be composed of any quaternary material that allows the desired

1 device performance. Also, in this preferred embodiment,
2 subcollector layer 30 is approximately 0.85 μm thick, which
3 allows low sheet resistance values (about 20 Ω/square).
4

5 The combination of using heavily doped InGaAsP of this
6 composition and a thick subcollector layer 30 allows the
7 achievement of low sheet and contact resistances needed for
8 high-speed device operation. The key reason for using the
9 transparent InGaAsP quaternary for the subcollector is that it
10 expands the optical mode in the vertical direction and thereby
11 increases the input mode coupling from commercially available
12 lensed optical fibers.
13

14 A collector layer 40 is epitaxially grown on subcollector
15 layer 30. In this preferred embodiment, collector layer 40 is
16 composed of undoped InGaAs and is approximately 0.4 μm thick.
17 The material comprising collector layer 40 is chosen such that
18 it absorbs the optical wavelengths of interest. It will be
19 understood that collector layer 40 can be composed of any
20 material that allows the desired device performance. The
21 thickness of the collector layer 40 is chosen to obtain the
22 desired transit frequency, breakdown voltage, base-collector
23 capacitance, and rate of optical absorption. The collector
24 layer 40 thickness of 0.4 μm allows transit frequencies of

1 approximately 130 GHz, which is needed for 40 Gbps data
2 transmission rates.

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4 A base region 50 is then epitaxially grown on collector
5 layer 40. In this preferred embodiment, the base region 50
6 consists of a heavily *p*-type doped InGaAs base region 60, which
7 is approximately 0.05 μm thick, onto which an undoped InGaAs
8 base layer 70 is epitaxially grown. Undoped InGaAs base layer
9 70 is approximately 50 Å thick. The thickness of the heavily
10 *p*-type doped InGaAs base region 60 was chosen as a tradeoff
11 between obtaining the desired base sheet resistance and base
12 transit time. An emitter region 80 is then epitaxially grown
13 on the undoped InGaAs base layer 70. The undoped InGaAs base
14 layer 70 acts as a spacer that reduces the amount of base
15 dopant diffusion into emitter region 80. Emitter region 80
16 consists of an *n*-type doped InGaAsP emitter layer 90 which is
17 approximately 0.1 μm thick onto which an *n*-type doped InP
18 emitter layer 100 is epitaxially grown. The *n*-type doped InP
19 emitter layer 100 is approximately 0.5 μm thick. The
20 composition of the *n*-type doped InGaAsP emitter layer 90 is
21 chosen so that the bandgap wavelength is approximately 1.15 μm ,
22 which is required to center the optical mode with collector
23 layer 40 and base region 50. Centering the optical mode
24 increases the rate of optical absorption.

1 An ohmic emitter contact layer 110 is then deposited onto
2 the *n*-type doped InP emitter layer 100. In this preferred
3 embodiment, the ohmic emitter contact layer 110 is composed of
4 heavily *n*-type doped InGaAs and is approximately 0.05 μm thick.
5 The thickness of the *n*-type doped InP emitter layer 100 is
6 chosen to prevent the optical mode from overlapping the ohmic
7 emitter contact layer 110 and causing unwanted optical loss
8 reducing the optical to electrical conversion efficiency of the
9 device.

10

11 It will be understood that many different configurations
12 can be used to produce the base and emitter regions, including
13 using multiple layers of various semiconductor alloys or by
14 using different doping configurations.

15

16 Finally, ohmic contacts need to be provided to ohmic
17 emitter contact layer 110, base region 60, and subcollector
18 layer 30. Ohmic contacts are made by etching the device down
19 toward the surface of the heavily *p*-type doped InGaAs base
20 region 60. This results in an emitter mesa of width, *W*, and
21 length, *L*. The width in the preferred embodiment is chosen to
22 be approximately 2 μm which allows for good input optical
23 coupling efficiency from commercially available lensed optical
24 fibers. The width could be made smaller to improve the speed

1 of the device, but this would reduce the input optical coupling
2 efficiency.

3
4 An ohmic emitter metallization region 140 and an ohmic
5 base metallization region 130 are formed on the ohmic emitter
6 contact layer 110 and the heavily *p*-type doped InGaAs base
7 region 60, respectively. In the preferred embodiment, the
8 ohmic emitter metallization region 140 and the ohmic base
9 metallization region 130 are comprised of a Ti/Pt/Au layer
10 structure. Ohmic emitter metallization region 140 is deposited
11 on the surface of the ohmic emitter contact layer 110 and the
12 heavily *p*-type doped InGaAs base region 60 using a standard
13 self-aligned metallization process. In short, the ohmic
14 emitter metallization region 140 and the ohmic base
15 metallization region 130 separate due to the slight undercut of
16 the emitter mesa and due to the ratio of the height of the mesa
17 to the thickness of the metallization. Ohmic base
18 metallization region 130 is self-aligned to the emitter region
19 80 to minimize the lateral extrinsic base resistance. A wet
20 etching technique is then used to etch collector layer 40 down
21 to subcollector layer 30. Ohmic base metallization region 130
22 behaves as a mask to the wet etching chemicals and causes an
23 undercut to be developed in collector layer 40. The undercut
24 allows a portion of the heavily *p*-type doped InGaAs base region
25 60 to extend out over subcollector layer 30. Ohmic base
26 metallization region 130 is then supported by the portion of

1 the heavily *p*-type doped InGaAs base region 60 that extends out
2 over subcollector layer 30. Undercutting the collector layer
3 40 minimizes the base-collector capacitance in the edge-
4 illuminated epilayer waveguide phototransistor 5. Reducing the
5 base-collector capacitance improves the speed of the device and
6 also makes the shape of the optical mode more circular, which
7 improves the input optical coupling efficiency.

8

9 An AuGe ohmic subcollector metallization layer 120 is then
10 deposited on subcollector layer 30. Subcollector layer 30 is
11 then etched down to substrate 10 to electrically isolate the
12 device. Subcollector layer 30, collector layer 40, base region
13 50, and emitter region 80 are formed so as to define an edge-
14 illuminated facet 145 for receiving incident light.

15

16 In addition to considering the electrical properties of
17 the edge-illuminated epilayer waveguide phototransistor 5, it
18 is necessary to consider the optical properties as well.
19 Collector layer 40 and base region 50 both serve as the region
20 of optical absorption. Hence, the thickness of collector layer
21 40 and base region 50 need to be such that all of the light is
22 absorbed after it impinges through the edge-illuminated facet
23 145 and travels down the length of collector layer 40 and base
24 region 50. A collector layer with thickness of 0.4 μm gives an
25 internal quantum efficiency of greater than 90% for collector

1 lengths approximately 7 μm . An internal quantum efficiency of
2 greater than 90% is sufficient for device operation.

3

4 Various changes and modifications to the embodiments
5 herein chosen for purposes of illustration will readily occur
6 to those skilled in the art. To the extent that such
7 modifications and variations do not depart from the spirit of
8 the invention, they are intended to be included within the
9 scope thereof which is assessed only by a fair interpretation
10 of the following claims.

11

12 Having fully described the invention in such clear and
13 concise terms as to enable those skilled in the art to
14 understand and practice the same, the invention claimed is: